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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,745	09/30/2003	Manu Gulati	BP3252	8011

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EXAMINER	
CHU, WUTCHUNG	

ART UNIT	PAPER NUMBER
2619	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,745	GULATI ET AL.	
	Examiner	Art Unit	
	Wutchung Chu	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,8,11,12,14 and 17-29* is/are rejected.

7)☒ Claim(s) *3,4,6,7,13,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This communication is in response to application's amendment filed on 8/27/2007. Claims 1-29 are pending.

Priority

2. Applicant's claim for domestic priority under 35 U.S. C. 119(e) is acknowledged.

Claim Rejections - 35 USC § 103

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 5, 8, 11-12, 14, and 17-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Calamvokis et al., hereinafter Calamvokis, (5592476) in view of Stacey et al., hereinafter Stacey, (US7020141).

Regarding claims 1 and 8, Calamvokis discloses asynchronous transfer mode switch with multicasting ability **(see Calamvokis col.3 line 63- col. 4 line 32)** comprising:

- receiving a data block at a receiver of the host device **(see Calamvokis col. 4 lines 3-5 receiving packets and col. 3 line 64 apparatus for receiving);**
- storing the data block in a receiver buffer **(see Calamvokis col. 4 lines 6-8 storage means for storing both the packet bodies of the packets received by the input means and queue data serving to identify in first-in-first-out order);**
- determining an input virtual channel corresponding to the data block **(see Calamvokis col. 4 line 4 the input identifier for the input stream to which the packet belongs);**
- determining an output virtual channel for the data block **(see Calamvokis col. 4 lines 23-29 output means for receiving from the send-control means the output identifier of the next scheduled output stream);**

Calamvokis discloses all the subject matter of the claimed invention with the exception of:

- updating an input virtual channel linked list corresponding to the input virtual channel to include the data block

- transferring the data block from the input virtual channel linked list of the receiver buffer to a destination within the host device via the output virtual channel;
- updating the input virtual channel linked list to remove the data block
- further comprising supporting a plurality of input virtual channel linked lists, wherein each input virtual channel linked list corresponds to a respective input virtual channel.

Stacey from the same or similar fields of endeavor teaches the use of queuing options for the AAL2 layer (or packet) queues are: 1) Per incoming link queues. AAL2 SDUs received over each individual input link to the ingress CPS are chained together into a single queue i.e. one link-list queue is maintained per serial link. **(see Stacey col. 6 line 23-25 and 39-54)**, and once stored the data remains in the same slot until the data is physically transmitted to the ATM network (via the ATM interface). Within the CPS, an SDU can be logically moved through the functional processes by simply transporting a pointer to the slot to the required process **(see Stacey col. 6 line 23-25 and 39-54),** and it is inherent that queue would remove the data block after transmission to destination.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the of queuing options for the AAL2 layer (or packet) queues as taught by Stacey in the asynchronous transfer mode switch with multicasting ability of Calamvokis in order to optimize buffering apportionment in order to minimize the delay

through any system and to minimize the memory and hence cost requirements of any implementation **(see Stacey col. 2 lines 15-19).**

Regarding claim 2, Calamvokis teaches determining an output virtual channel **(see Calamvokis col. 4 lines 20-22 the output streams on the basis of the output identifiers and indicating the next scheduled output stream by outputting the corresponding output identifier)** for the data block includes processing one or more of the input virtual channel **(see Calamvokis col. 3 line 63 at least one input stream of packets)**, a header corresponding to the data block, a protocol corresponding to the data block, source identifier/address corresponding to the data block, and a destination identifier/address corresponding to the data block **(see Calamvokis figure 1).**

Regarding claim 5, Calamvokis teaches comprising writing a data block to the receiver buffer **(see Calamvokis col. 26 lines 24-25 and col. 4 lines 6-14)** and reading a data block from the receiver buffer **(see Calamvokis col. 26 lines 51-53 a read from the FIFO)** in a single read/write cycle **(see Calamvokis col. 26 lines 20-55 shows the procedure of writing and reading)**.

Regarding claim 9, Calamvokis teaches further comprising supporting a free linked list that includes a plurality of vacant data blocks of the receiver buffer **(see column7 line 52 , and col. 13 lines 26-28)**.

Regarding claim 10, Calamvokis teaches further comprising maintaining a mapping indicating a relationship between a plurality of input virtual channels and a plurality of output virtual channels **(see col. 13 line 16-20)**.

Regarding claims 11 and 17, Calamvokis teaches a method for routing data within a host device comprising:

- receiving a data block at a receiver of the host device **(see Calamvokis col. 4 lines 3-5 receiving packets and col. 3 line 64 apparatus for receiving)**, the data block received via an input virtual channel **(see Calamvokis col. 11 lines 27-29)**;

- storing the data block in a receiver buffer **(see Calamvokis col. 4 lines 6-8 storage means for storing both the packet bodies of the packets received by the input means and queue data serving to identify in first-in-first-out order)**;

- when the input virtual channel has identified therewith an output virtual channel updating an output virtual channel linked list corresponding to the output virtual channel to include the data block **(see Calamvokis col. 4 lines 65 – col. 5 line 2)**; and

- when the input virtual channel has not identified therewith an output virtual channel **(see Calamvokis col. 5 lines 19-24)**:

    - processing the data block to determine an output virtual channel for the data block **(see Calamvokis col. 7 lines 57-59)**;

- updating an output virtual channel linked list corresponding to the output virtual channel to include the data block **(see Calamvokis col. 5 lines 34-41)**; and

Calamvokis discloses all the subject matter of the claimed invention with the exception of:

- updating an input virtual channel linked list corresponding to the input virtual channel to include the data block;
- updating the input virtual channel linked list to remove the data block
- further comprising supporting a plurality of input virtual channel linked lists, wherein each input virtual channel linked list corresponds to a respective input virtual channel.

Stacey from the same or similar fields of endeavor teaches the use of queuing options for the AAL2 layer (or packet) queues are: 1) Per incoming link queues. AAL2 SDUs received over each individual input link to the ingress CPS are chained together into a single queue i.e. one link-list queue is maintained per serial link. **(see Stacey col. 6 line 23-25 and 39-54)**, and it is inherent that queue would remove the data block after the transmission of data packet to destination. The AAL2 layer queuing function is maintained by implementing a number of linked-lists **(see Stacey col. 7 lines 4-7)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the of queuing options for the AAL2 layer (or packet) queues as taught by Stacey in the asynchronous transfer mode switch with multicasting ability of

Calamvokis in order to optimize buffering apportionment in order to minimize the delay through any system and to minimize the memory and hence cost requirements of any implementation **(see Stacey col. 2 lines 15-19).**

Regarding claim 12, Calamvokis teaches further comprising:

- transferring the data block from the receiver buffer to a destination within the host device based upon a corresponding output virtual channel **(see Calamvokis col. 4 lines 40-49)**; and
- updating the output virtual channel linked list to remove the data block **(see Calamvokis col. 4 lines 20-22)**.

Regarding claim 14, Calamvokis teaches comprising writing a data block to the receiver buffer **(see Calamvokis col. 26 lines 24-25 and col. 4 lines 6-14)** and reading a data block from the receiver buffer **(see Calamvokis col. 26 lines 51-53 a read from the FIFO)** in a single read/write cycle **(see Calamvokis col. 26 lines 20-55 shows the procedure of writing and reading)**.

Regarding claim 18, Calamvokis teaches comprising supporting a plurality of output virtual channel linked lists, wherein each output virtual channel linked list corresponds to a respective output virtual channel **(see Calamvokis col. 32 line 60 – col.33 line 9).**

Regarding claim 19 Calamvokis teaches further comprising supporting a free linked list that includes a plurality of vacant data blocks of the input buffer **(see Calamvokis col. 9 lines 11-21).**

Regarding claim 20, Calamvokis teaches a received data processing and storage system **(see Calamvokis col. 3 lines 62-67)** comprising:

- an input that receives data blocks corresponding to a plurality of input virtual channels **(see Calamvokis col. 3 lines 62-67)**;
- a routing module that determines an output virtual channel for data blocks based upon their respective input virtual channels **(see Calamvokis col. 3 lines 62- col 4 line2)**;
- a receiver buffer operable to instantiate an input virtual channel linked list for storing data blocks on an input virtual channel basis and to instantiate a free list that identifies free data locations **(see Calamvokis col. 4 lines 6-8 storage means for storing both the packet bodies of the packets received by the input means and queue data serving to identify in first-in-first-out order, and col. 9 lines11-21 free address list)**;
- a linked list control module operably coupled to the receiver buffer **(see Calamvokis col. 4 lines 30-40)**;
- free linked list registers operably coupled to the linked list control module **((see Calamvokis col. 4 lines 15-22 and 41-50 send-control means and col. 9 lines11-21 free address list)**.

Calamvokis discloses all the subject matter of the claimed invention with the exception of:

- input virtual channel linked list registers operably coupled to the linked list control module; and

Stacey from the same or similar fields of endeavor teaches the use of queuing options for the AAL2 layer (or packet) queues are: 1) Per incoming link queues. AAL2 SDUs received over each individual input link to the ingress CPS are chained together into a single queue i.e. one link-list queue is maintained per serial link. **(see Stacey col. 6 line 23-25 and 39-54)**, and queue manager device **(see Stacey col. 4 line 56)**.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the of queuing options for the AAL2 layer (or packet) queues as taught by Stacey in the asynchronous transfer mode switch with multicasting ability of Calamvokis in order to optimize buffering apportionment in order to minimize the delay through any system and to minimize the memory and hence cost requirements of any implementation **(see Stacey col. 2 lines 15-19).**

Regarding claim 21, Calamvokis teaches further comprising an output that transmits data blocks **(see Calambokis col.4 lines 24-29 outputting the retriveved packet body on the scheduled output stream, and figure 4 ref37 input port)** and discloses all the subject matter of the claimed invention with the exception of corresponding to a plurality of input virtual channels. It would have been obvious to one of ordinary skill in the art at the time of the invention to include an output that transmits data blocks corresponding to a plurality of input virtual channels since Calamvokis teaches different service such as guaranteed bandwidth and best effort **(see Calambokis col. 29 lines 24-49)** and inputs are associated with their services. These

inputs are scheduled for transmission to a particular VCN, which outputting packets can be of a plurality of inputs/services.

Regarding claim 22, Calamvokis teaches wherein:

- the receiver buffer is further operable to instantiate an output virtual channel linked list for storing data blocks on an output virtual channel basis **(see Calamvokis col. 4 lines 6-14 storage means for storing both the packet bodies of the packets received by the input means and queue data serving to identify in first-in-first-out order and col. 4 lines 65-57 forming a list)**; and

- the system further comprises output virtual channel linked list registers **(see Calamvokis col. 4 lines 65-57 forming a list)** operably coupled to the linked list control module **(see Calamvokis col. 4 lines 24-29 output means)** and an input virtual channel to output virtual channel map **(see Calamvokis col. 13 lines 21-28)**.

Regarding claim 23, Calamvokis teaches the receiver buffer comprises:

- a pointer memory **(see Calamvokis col. 4 lines 30-40 injection means)**; and

- a data memory, wherein a single address addresses corresponding locations of the pointer memory and of the data memory **(see Calamvokis col. 4 lines 6-14)**.

Regarding claim 24, Calamvokis teaches the receiver buffer further comprises a packet status memory, wherein a single address addresses corresponding locations of the pointer memory **(see Calamvokis col. 33 line 60 and col. 34 line 5 head pointer)**, the data memory **(see Calamvokis col. 4 lines 6-14)**, and the packet status memory **(see column 33 line 47-49)**.

Regarding claim 25, Calamvokis teaches further comprising a pointer memory read port **(see Calamvokis col. 26 line 41 read pointer)**, a pointer memory write port **(see Calamvokis col. 26 line 32 write pointer)**, a data memory read port **(see Calamvokis col. 26 line 40 reading)**, and a data memory write port **(see Calamvokis col. 26 line 25 writing)**, each of which can access the receiver buffer in a common read/write cycle **(see Calamvokis col. 26 lines 20-55 shows the procedure of writing and reading)**.

Regarding claim 26, Calamvokis teaches wherein:

a single pointer memory location can be read from and written to in a common read/write cycle **(see Calamvokis col. 26 line 42-45)**; and a single data memory location can be read from and written to in a common read/write cycle **(see Calamvokis col. 25 line 54)**.

Regarding claim 27, Calamvokis teaches wherein the receiver buffer comprises:

- a pointer memory **(see Calamvokis col. 4 lines 30-40 injection means)**;
- a data memory **(see Calamvokis col. 4 lines 6-14)**;

- a packet status memory **(see column 33 line 47-49)**; and
- wherein a single address addresses corresponding locations of the pointer memory, the data memory, and the packet status memory **(see Calamvokis col. 4 lines 4 input identifier)**.

Regarding claim 28, Calamvokis teaches further comprising:

- a pointer memory read port **(see Calamvokis c. 26 line 41 read pointer)**;
- a pointer memory write port **(see c. 26 line 32 write pointer)**;
- a data memory read port **(see Calamvokis col. 26 line 40 reading)**;
- a data memory write port **(see Calamvokis col. 26 line 25 writing)**;
- a packet status memory read port **(see Calamvokis col. 31 line 35 retrieves the cell-details for the next-to-be-sent cell)**; and
- a packet status memory write port **(see Calamvokis col. 30 lines 39-40)**.

Regarding claim 29, Calamvokis teaches wherein:

- a single pointer memory location can be read from and written to in a common read/write cycle (**see Calamvokis col. 26 line 42-45)**;
- a single data memory location can be read from and written to in a common read/write cycle **(see Calamvokis col. 25 line 54)**; and

- a single packet status memory location can be read from and written to in a common read/write cycle **(see Calamvokis col. 31 line 35 retrieves the cell-details for the next-to-be-sent cell, and col. 30 lines 39-40)**.

Allowable Subject Matter

6. Claim3-4, 6-7, 13, and 15-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments, see page 10 of the remarks, filed 8/27/2007, with respect to claim 12 have been fully considered and are persuasive. The objection of claim 12 has been withdrawn.

8. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Branth et al. (US6822958)

Osborne et al. (US5751951)

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Wutchung Chu whose telephone number is 571 270 1411. The examiner can normally be reached on Monday - Friday 1000 - 1500EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan D. Orgad can be reached on 571 272 7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WC/
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